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SPICE-Compatible Behavior Model of Multiphase Voltage Regulator Module for End-to-End Power Integrity Simulation

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Abstract

Accurate end-to-end power integrity simulations require models that include every component in the power distribution network (PDN), from voltage regulator modules (VRMs) all the way to on-die capacitors. However, including VRM modules in power integrity simulations has been challenging because SIMPLIS is not compatible with typical power integrity simulation tools (e.g., HSPICE), and encrypted VRM models for SPICE tools are typically not accurate enough to capture the voltage droop under various load conditions. Moreover, simple resistor-inductor networks fail to capture the nonlinear behavior of the PDN. In this paper, we propose a SPICE-compatible behavior modeling method, which we apply and validate for a practical multiphase VRM in a mobile platform. Our model adequately captures the control loops of the VRM, such as single-voltage and multiple current feedback loops. By combining the parameter-based equations from the voltage and current feedback networks, the model also reproduces pulse-width modulation-based VRM operation. For the validation of the behavior model, the design parameters are determined following a two-step process proposed here. Finally, the proposed behavior modeling method is experimentally validated using an evaluation board with various load conditions.

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Lihui Cao received a Ph.D. in electrical engineering from Rutgers University (New Jersey, USA). He worked with Apple, Broadcom, and LSI as a design engineer and signal and power integrity engineer for more than 20 years. He then joined Google's consumer product silicon group and is currently working as the signal and power integrity team manager.

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I. Introduction

Power distribution networks (PDNs) are important for state-of-the-art applications ranging from laptops to mobile platforms. Providing a reliable power supply for a device requires optimization of the PDN and end-to-end power integrity (PI) analysis. As shown in Fig. 1, a hierarchical PDN can be divided into several parts: the voltage regulator module (VRM), printed circuit board (PCB), package, and on-chip PDN. When the load application demands a transient current on the on-chip die bump, a voltage droop can occur. This time-domain voltage droop is strongly associated with the impedance of the hierarchical PDN and the current supply from the VRM. It is therefore essential to include information on every component of the PDN, from the VRM all the way to the on-chip PDN, for accurate end-to-end PI simulation.

Modeling of PCB- and package-level PDN design have already been widely researched. According to previous studies, the PDN can be modeled using various combinations of power/ground shapes, capacitors, and passive components in conventional 3D simulators. The 3D PDN models in the frequency domain can then be exported and imported to other platforms as S-parameters blocks. However, PI analysis that includes the VRM is still challenging and has been the subject of several recent studies.

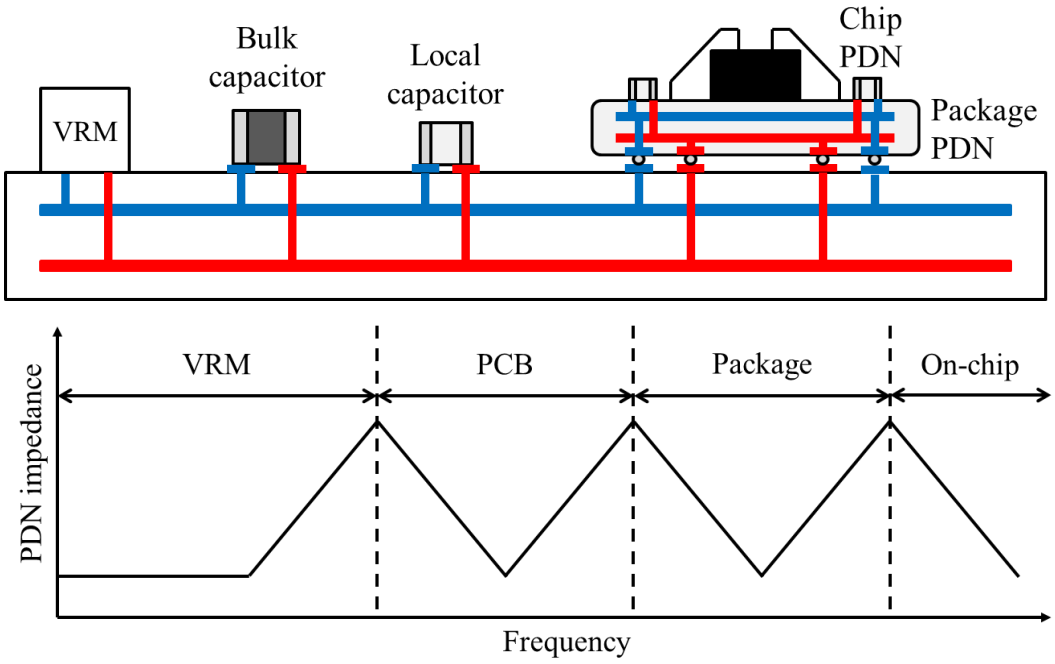

Fig. 1. Simplified printed circuit board (PCB), including a voltage regulator module (VRM).

The simplest methods for modeling the VRM are the first-order resistor-inductor (RL) model and the four-element RL model [1]. The four-element RL model relies on simple equations that were derived to describe the voltage droop, and resistance and inductance are both fitted with the measured voltage waveforms. However, the passive components in these models cannot fully capture the non-linear behavior of VRMs. To overcome the drawbacks of linear VRM models, many studies use the encrypted VRM model provided by the manufacturer and an accurate simulation model of the VRM in SIMPLIS, which

includes the complex control loops and parasitics of the PCB and on-chip PDN. Nevertheless, the limited flexibility of encrypted VRM models and the SPICE-compatibility issue of SIMPLIS models allow for only a few options when running PI simulations to optimize PCB designs. Thus, simple behavior modeling methods for the VRM are used to improve both the non-linearity and flexibility of simulation models. For example, Baek et al. [2] modeled a boost converter with a simplified feedback control loop. Other studies have modeled combined buck/boost converters operating in continuous and discontinuous conduction modes (CCM and DCM) [3-4]. However, these studies only consider a single voltage loop, but the recent VRMs use dual control loops with current feedback networks.

Another study proposed a consolidated modeling method for complex VRMs [5]. In this approach, a small signal model for CCM, and for the DCM in a pulse-width modulated (PWM) converter, is generated using the number of design parameters. The input-to-output impedance, power supply rejection ratio (PSRR), and properties of each voltage and current control loop are then modeled theoretically based on the VRM design parameters. For this modeling method, the loop gain in the frequency domain is measured and the relevant design parameters are fitted. The operational transconductance amplifier (OTA)-based large signal circuit is used to implement the small signal models. The properties of the OTA model are validated with the measured bode plots. By combining the small and large signal models with circuit-based error amplifiers, the consolidated VRM model is applied in the advanced design system (ADS). The model can effectively reproduce CCM, DCM in a PWM converter, the input and output impedance of the VRM, and slope compensation to improve PSRR. The S-parameters compatibility of the ADS also allows for electromagnetic analysis. However, the complexity of OTA circuits and the model validation process make this method unattractive. Furthermore, the sophisticated features of VRMs, such as pulse frequency modulation and automatic current shedding and addition, are not modeled accurately in this modeling approach.

In this paper, a SPICE-compatible behavior modeling method is proposed. The method is applied to a practical multiphase VRM in a mobile platform and successfully validated. The control loops of the VRM, including a single voltage and multiple current feedback loops, are all captured in this model. A parameterized equation-based model of the PI controller is used to mimic the general voltage feedback loop. By optimizing the parameters of the PI controller in the behavior model, the simulation captures the function of any controller in the voltage feedback loop. The parameter-based equations of peak current mode control topology are derived for the current feedback loop. By combining the parameter-based equations from voltage and current feedback network, a pulse width modulation (PWM)- based VRM operation is reproduced. The proposed parameter-based equations and external passive components of VRM circuits are then combined, and the time-continuous control signal is generated from the VRM control loops. Because of the continuous-time signal, the time required for transient analysis is substantially less than for the typical switching-based simulation models.

The proposed behavior modeling method is experimentally validated using an evaluation board (EVB) with multiple load conditions. The target EVB is composed of single-phase and three-phase VRMs which are integrated into a single power management integrated circuit. A built-in load slammer circuit on the EVB is used to control the load

current. Our proposed behavior model, run under the forced PWM model, measures and reproduces the sophisticated features of single- and multiphase VRMs.

II. Behavior Modeling of Single and Multiphase VRMs

VRMs may be different in a wide range of chip and package designs, and step-down buck converters are usually used to handle the heavy current on the power rail. Fig. 2 shows a typical buck converter. The input voltage V_{in} is regulated by the high- and low-side metal-oxide-semiconductor field-effect transistor (MOSFET) switches. The built-in controllers, including PI, comparator, and set-reset flip-flop controllers generate alternating on-off signals with the switching frequency F_{SW}, and the duty cycle D to excite the gate driver of both MOSFET switches. The switching node V_{SW} is then connected to the external inductor L and the bulk output capacitor C_{out} to produce the smooth DC output voltage V_{out}.

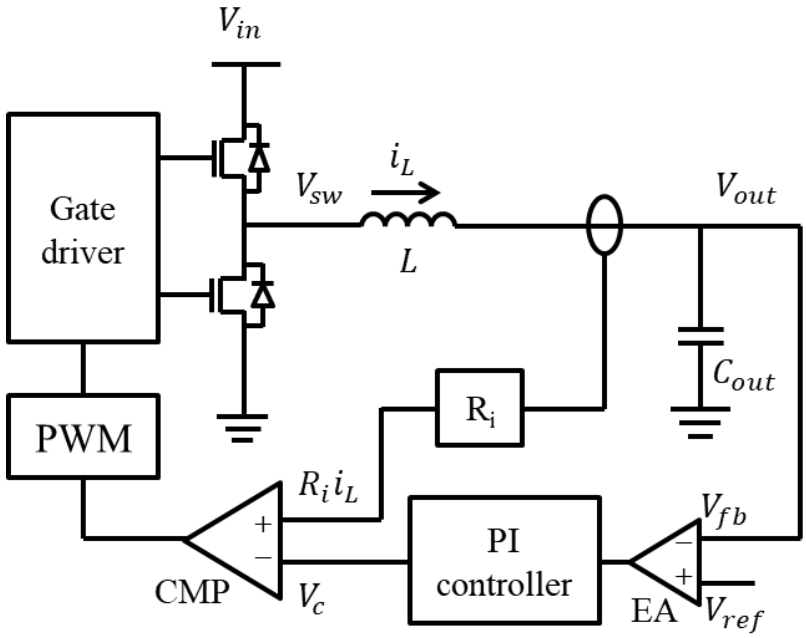

Fig. 2. Block diagram of current-mode buck converter.

To minimize the undershooting and overshooting of voltages during the transient response, the number of control loops is integrated into the buck converters. A single voltage feedback loop with voltage-mode control is widely used due to its simplicity and ease of implementation. However, a critical drawback of this system is the lack of loop gain and the limited bandwidth. Recent designs have proposed an additional current feedback loop for stable voltage regulation. As a result, the current-mode control feature is mainly used as the control scheme of VRMs.

Fig. 2 depicts the typical current-mode control topology, with dual voltage and current feedback loops. With the remote sensing function, the voltage feedback loop senses the output voltage as close to the current load as possible. The sensed voltage is compared with the internal voltage level V_{ref} to generate the error signal, which is then forwarded to the PI controller. The output of the PI controller V_C and the feedback current with the current-

sensing gain R_i are used as inputs for the comparator. Finally, the set-reset flip-flop, which is synchronized with the clock frequency, generates the turn-on signals with the duty cycle of D to turn the MOSFET switches on and off.

With the various controllers, the DC output voltage is determined by the input voltage and its duty cycle: $V_{out} = V_{in}D$ [6]. To reproduce an identical output voltage in the simulation model, it is therefore important to generate the appropriate duty cycle. In the following sections, we introduce parameter-based equations to describe the generic behavior of a buck converter. We also propose the basic operation of single-phase and complex multiphase buck converters.

A. Single-Phase VRM

For the completeness of this paper, we briefly reiterate the modeling method of a PWM-based single-phase buck converter under CCM in this section. We propose a simulation model based on the behavior of the inductor current. The design parameters-based equations allow the behavior of the target buck converters to be updated, which makes the PI simulation extremely flexible. The simulation can be even further improved to mimic sophisticated features such as pulse frequency modulation, load line calibration, and automatic phase drop/add (APD); these improvements are achieved by updating the proposed parameter-based equations.

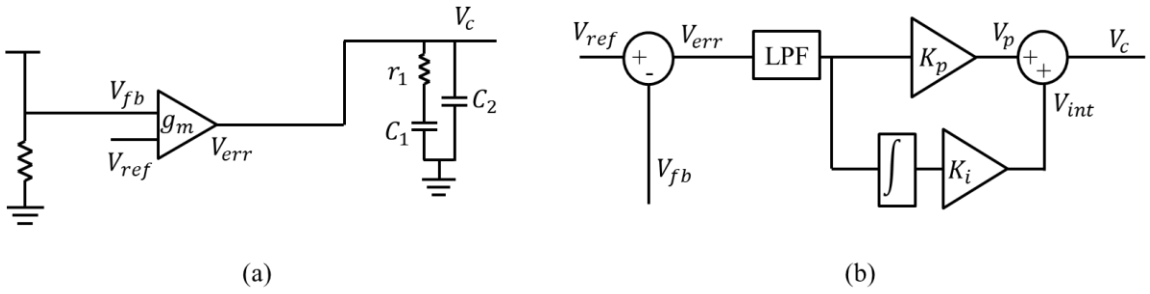

Fig. 3. PI controller in a voltage loop. (a) PI circuit; (b) block diagram of PI controller.

Fig. 3 shows a typical voltage feedback loop. The voltage control loop is fed by the feedback voltage V_{fb}; the error voltage V_{err} is subsequently generated. The transconductance g_m of the error amplifier converts the V_{err} to i_C and excites the PI controller described in resistor-capacitor circuits. It is convenient to derive the PI controller with S-domain analysis. The combination of resistor-capacitor circuits in the block diagram is shown in Fig. 3(b), and the associated transfer function is as follows:

$$\frac{V_C}{V_{err}} = \frac{g_m(sC_1r_1 + 1)}{s^2C_1C_2r_1 + s(C_1 + C_2)}. \tag{1}$$

In practical buck converter designs, $C_1 \gg C_2$ when a large capacitor C_1 provides the low-frequency pole of the current-mode topology, and C_2 adds a high-frequency pole to block the high-frequency noises. Thus, (1) can be even further simplified to:

$$\frac{V_C}{V_{err}} \approx \frac{1}{sC_2r_1 + 1}\left(g_mr_1 + \frac{g_m}{C_1}\frac{1}{s}\right). \tag{2}$$

The right-hand side of (2) contains the low-frequency pole described by $C_2 r_1$ and design parameters for the PI controller. The cut-off frequency of the low-pass filter shown in the first term in (2) can be described by:

$$f_c = \frac{1}{2\pi C_2 r_1}. \tag{3}$$

The second term in (2) is used as the PI controller gain of K_P and K_I as

$$K_P = g_m r_1 \tag{4}$$

$$K_I = \frac{g_m}{C_1} \tag{5}$$

where K_P and K_I are the proportional and integrator gain of the voltage feedback loop, respectively. In the actual design, the integrator cannot have infinitely large gain, the gain of the integrator is limited by the DC gain limitation K_{DC}. Finally, the voltage control loop can be derived with the parameter-based equation as follows:

$$\frac{V_C}{V_{err}} \approx \frac{1}{sC_2 r_1 + 1}\left(k_p + \frac{K_{DC}}{\frac{sK_{DC}}{K_I} + 1}\right). \tag{6}$$

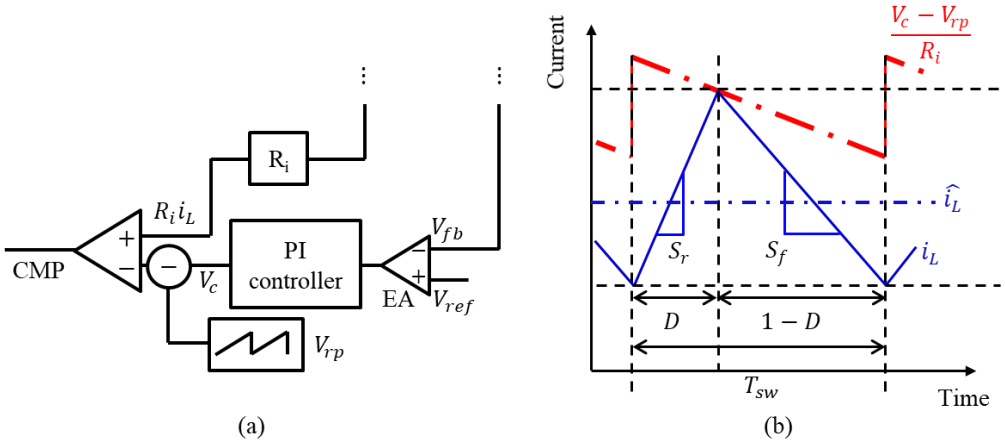

Fig. 4. Current loop of simulation model (a) Comparator circuit in the model. (b) Inductor current behavior.

Fig. 4 shows both the comparator fed by the inductor current i_L and the output of the PI controller V_c. Within each switching cycle T_{sw}, the averaged inductor current $\widehat{i_L}$ is calculated to replace the switching nature of MOSFETs with continuous time behavior. In the proposed simulation model, the behavior of the PWM generator circuit is solved for the duty cycle D based on the design parameters [7]. The design parameter-based duty cycle can be described by:

$$D = \frac{1}{2} + \frac{V_{rp}}{T_{sw}\Delta S R_i} - \sqrt{\left(\frac{1}{2} + \frac{V_{rp}}{T_{sw}\Delta S R_i}\right)^2 - \frac{2}{T_{sw}\Delta S}\left(\frac{V_C}{R_i} - \widehat{i_L}\right)} \tag{7}$$

where V_{rp} and R_i are the ramp voltage for slope compensation and the current sensing gain, respectively. We define ΔS as the difference between the rising and falling slopes of the inductor current:

$$\Delta S = \frac{V_{in} - \hat{\imath}_L(r_{on,H} + r_L) - V_{out}}{L} + \frac{\hat{\imath}_L(r_{on,L} + r_L) - V_{out}}{L} \quad (8)$$

where $r_{on,H}$ and $r_{on,L}$ are the turn-on resistance of high- and low-side MOSFETs, respectively, and r_L is the DC resistance of the external inductor. Using the duty cycle defined in (7) and (8), the average inductor current $\hat{\imath}_L$ can finally be generated in a continuous time waveform.

Fig. 5 shows the HSPICE implementation of (7) and (8). Specifically, the code in Fig. 5 shows that the behavioral voltage sources are used to describe the changing variables ΔS and $\hat{\imath}_L$ as *E_TSDS* and *v(cursen)*, respectively. The duty cycle D is implemented as *E_dtc* using the design parameters and variables. Later in this article, we will apply this voltage source to another behavior source to mimic the switching node voltage $\widehat{V_{sw}}$.

```
E_sr sr gnd vol='(V_in-(R_hmos+R_L)*v(cursen)-v(out))/L_ind'
E_sf sf gnd vol='((R_lmos+R_L)*v(cursen)-v(out))/L_ind'
E_TSDS tsds gnd vol='(v(sr)-v(sf))/F_s'
E_dtc dtc gnd vol='min(max((0.5+(V_ramp/(v(tsds)*R_i)))-sqrt(((0.5+(V_ramp/(v(tsds)*R_i)))^2)
-(2/v(tsds))*((v(vpi)/1/R_i)-(v(cursen)/1^2))),0),1)'
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Fig. 5. HSPICE implementation using behavioral voltage sources.

B. Multiphase VRM

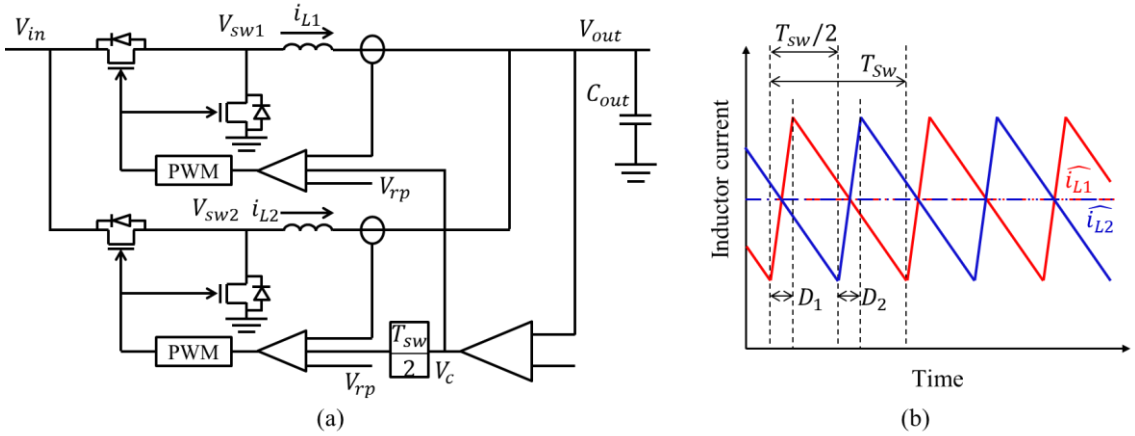

Fig. 6. Multiphase VRM (a) block diagram and (b) averaged waveforms.

A simple block diagram for a multiphase VRM is depicted in Fig. 6(a). In this case, double-phase VRM is used to describe the multiphase operation. As shown in Fig. 6(a), a multiphase VRM typically has a single voltage loop and multiple current loops for each phase. For the secondary phase, a time delay of $T_{sw}/2$ is used to represent the alternate switching behavior of the primary and secondary phases. The inductor current behavior of the secondary phase is therefore delayed by $T_{sw}/2$ in the proposed simulation model. An identical equation for the single voltage loop (6) is applied to the simulation model. Then, the duty cycle expression (7) described by D_1, and D_2 for each phase can be generated with the multiple current loops combined with a single voltage loop. For the HSPICE implementation, the same behavioral voltage sources with the time delay $T_{sw}/2$ is applied on the voltage loop for the secondary phase.

III. Parameter Optimization and VRM Modeling

In this section, the modeling of VRM, and design parameters extraction and tuning methods are introduced. Because the switching behavior controlled by duty cycle D is simplified by an equation, the proposed model generates time-continuous waveforms. With the continuous time VRM model, the resource consumption of transient analysis is greatly reduced.

A. Single and Multiphase VRM Modeling

The proposed continuous time simulation model is shown in Fig. 7. To ensure the flexibility and simplicity of the simulation model, the complex controllers are replaced by an equation-based user-defined voltage source. The user-defined voltage-controlled voltage source (VCVS) replicates the averaged switching node voltage $\widehat{V_{sw}}$, which is described as:

$$\widehat{V_{sw}} = D\left(V_{in} - r_{on,H}\widehat{i_L}\right) - (1-D)r_{on,L}\widehat{i_L}. \tag{8}$$

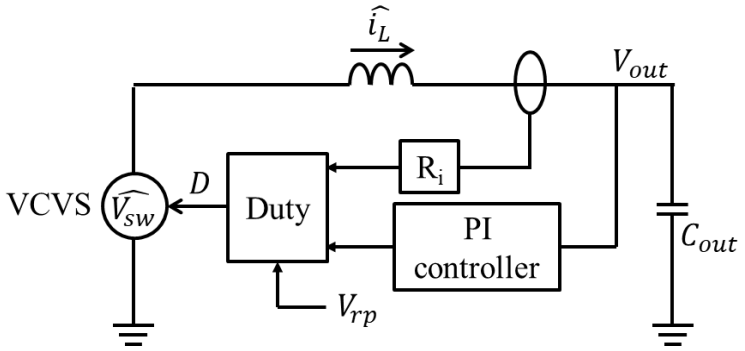

Fig. 7. Proposed continuous-time single-phase VRM model.

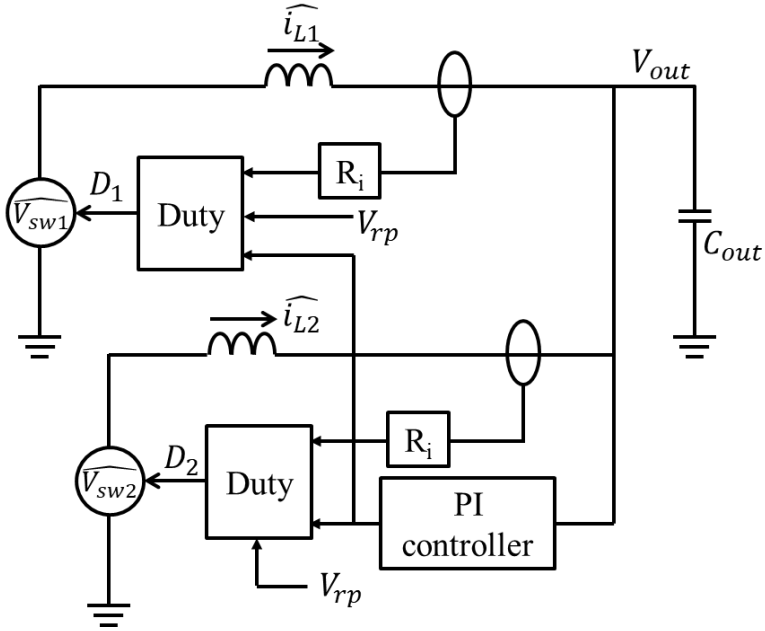

Fig. 8. Proposed continuous-time multiphase VRM model.

Because the mandatory parameters of the voltage and current control loops in (7) are already embedded in *D*, the proposed model can be utilized to mimic the PWM- and CCM-based current-mode VRMs. By updating the design parameters in (1) – (8), the various transient responses can be replicated depending on the load current conditions. The rest of the buck converter circuits, including the inductor and capacitor, can be applied followed by the voltage source.

The proposed model can be extended to the multiphase VRMs. As shown in Fig. 8, two user-defined voltage sources represent the averaged switching node voltage for primary and secondary phases. To run the behavior model for a multiphase system, the switching delay $T_{sw}/2$ is applied to the PI controller for the secondary phase. The resulting multiphase VRM model adequately reproduces the simple transient response of multiphase VRMs.

In addition, the multiphase behavior model can be further improved to mimic complex multiphase VRM features such as APD, dynamic current sharing for DC current stabilization, and load line calibration. For example, APD can easily be implemented in the simulation model: because the number of activated phases in multiphase VRMs is determined by the load current and the phase add/drop threshold, the load dependent PI controller is implemented in the simulation model. To mimic this feature, the PI controller in the single voltage loop of Fig. 8 is replaced with a load-dependent PI controller. Two different design parameter sets for the PI controller specified in (6) are used for single- and double-phase operations of the VRM. The load-dependent PI controller then selects a parameter set based on the amplitude of load current. Under "light loading" conditions, the switching node of the secondary phase is shorted to the output because the MOSFET switches are turned off. Thus, the output voltage V_{out} must be included in the VCVS in (8) for the secondary phase behavior under light loading conditions. Finally, the APD can be implemented in the HSPICE-based simulation setup by updating the control blocks and analytical equations depending on the loading condition of the multiphase VRM. Detailed methods for the sophisticated features of multiphase VRMs will be introduced in future publications.

B. Two-Step Parameter Optimization

Table 1. Design parameters of the proposed behavior model

Type	Parameters	Description
Known parameters	L	External inductor
	C_{out}	Output capacitor
	$r_{on,H}, r_{on,L}$	Turn-on resistance of switches
	r_L	DC resistance of inductor
	V_{ref}	Reference voltage
	V_{in}	Input voltage
	T_{sw}	Switching period

Extracted and tuned parameters	R_i	Current sensing gain
	V_{rp}	Ramp compensation voltage
	K_{DC}, K_P, K_I	Parameters for PI controller
	f_c	Cutoff frequency of low pass filter

To extract and tune the internal circuit parameters, a two-step method is proposed [8]. Table 1 summarizes the design parameters for the model, which are divided into the two sections of the proposed simulation model (known parameters and the extracted and tuned parameters). The known parameters are provided by the manufacturer or can be found on the circuit datasheet. In contrast, the extracted and tuned parameters are applied to the simulation setups to replicate the behaviors of internal controllers in (1) – (8). The four unknowns are separated into DC parameters and AC parameters. The two-step method involves determining and fine-tuning the DC and AC parameters, respectively.

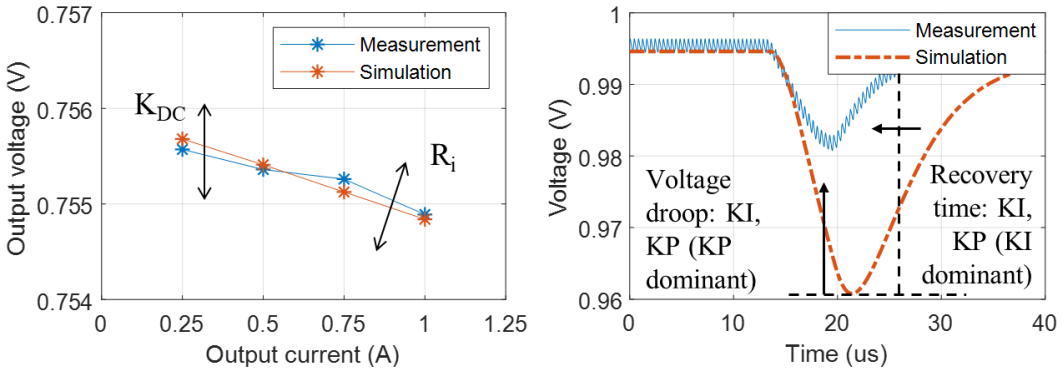

Fig. 9. Two-step parameter optimization: (a) extracting DC parameters; (b) tuning AC parameters

The measurement-based extraction and tuning methods are shown in Fig. 9, which indicates that the DC and AC parameters determine the steady-state and step response of the proposed model. To extract the DC parameters, the output voltage is measured as a function of the constant load current. The resulting I-V curve is mainly described by the DC gain limitation K_{DC} and the current-sensing gain R_i. Based on the extracted data, the DC offset, and the slope of the I-V curve are determined by K_{DC}, and R_i, respectively. For example, the K_{DC} in the PI controller of the voltage feedback loop determines the DC offset under the specific loading condition. The DC parameters for the simulation model can be updated using the I-V curve of the target VRM measurement results until the simulated and measured I-V curves show a good correlation. As shown in Fig. 9(b), the step response of the VRM is mainly determined by the AC parameters, including the PI controller parameters K_p and K_I. For example, in the PI controller of the voltage feedback loop, the initial droop level and the stability of the step response are significantly affected by the proportional gain K_p. The integral coefficient K_I mainly affects the recovery time of the voltage droop in the step response of the VRM. To capture the full characteristics of both steady and step responses of the target VRM, extraction and tuning of both the DC and AC parameters must be performed carefully. The goal of the two-step method described here

is to minimize any transient errors between the measured and simulated output voltage waveforms, within a given time frame, by optimizing the design parameters.

IV. Validation

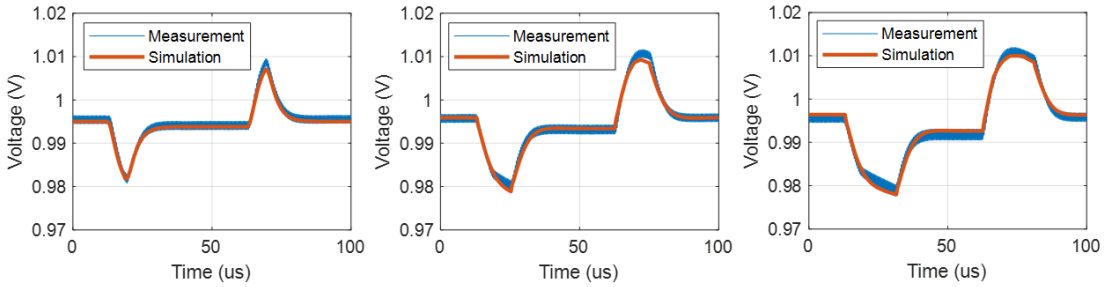

Fig. 10. Correlation results between simulation and measurement for a single-phase VRM with a load of (a) 1–2 A; (b) 1–3 A; and (c) 1–4 A.

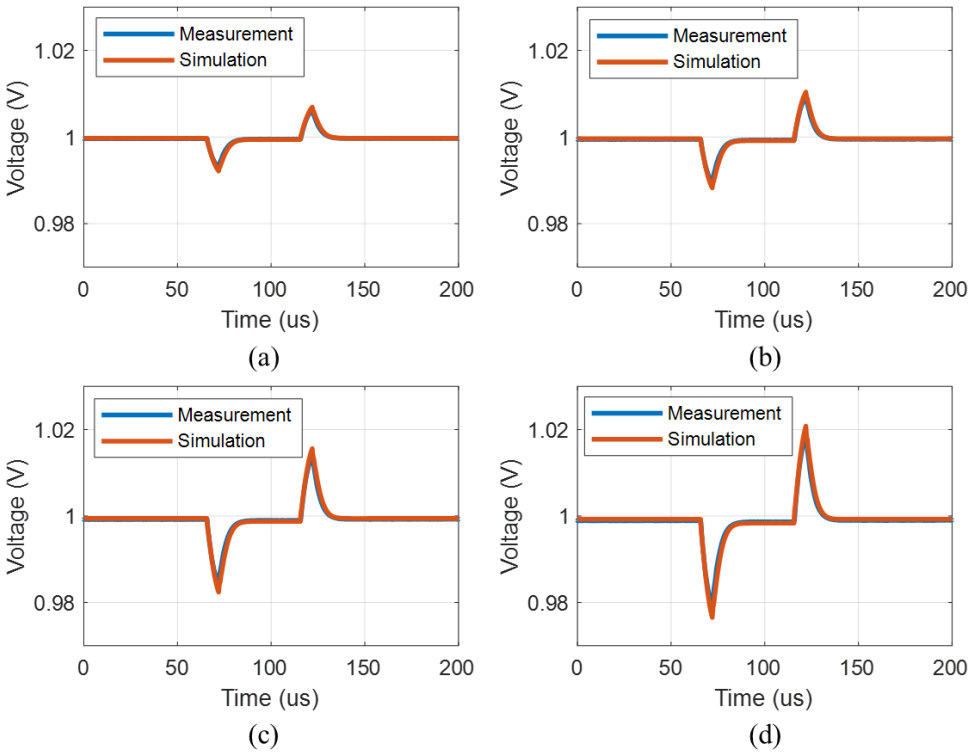

Fig. 11. Correlation results between simulation and measurement for a three-phase VRM with a load of (a) 2–3 A / 5 µs; (b) 2–5 A / 5 µs; (c) 2–8 A / 5 µs; and (d) 2–10 A / 5 µs.

The proposed continuous time modeling method is validated for both single- and three-phase buck converters. First, the output voltage waveforms under various load current conditions are measured. The waveforms simulated with the optimized design parameters are then compared to the measurement results for both single- and three-phase VRMs. The input voltage for the single-phase VRM is 4 V, and the output voltage is 1 V. By gradually increasing the amplitude of step load current from 2–4 A with the 200 mA / µs of slew-rate injected by load slammer, various output voltages are measured. The measurement and

simulation results are shown in Fig. 10. Overall, the measured and simulated voltage waveforms show good correlations regardless of the loading conditions. The maximum correlation error occurred at the 1–3 A loading condition with an input voltage of 4 V; for this condition, measured result overshot the simulated voltage by 2.1 mV.

Fig. 11 shows the measurement validation for the three-phase VRM. For these measurements, the input voltage is 4 V, and the output voltage is configured to be 1 V. To ensure full-phase operation, the minimum loading current is set at 2 A. Because the fixed slew-rate cases are validated in Fig. 10, the transient responses under different step amplitude with different slew-rates are compared in this step. As shown in Fig. 11, the measured and simulated results for three-phase operations also show good correlations under various situations.

To further validate the proposed modeling method, the complex multiphase operation is tested. For this test, the APD operation of three-phase VRM is compared. The APD is widely used in a multiphase VRM to reduce the power loss under lighter load conditions. The three-phase VRM has hysteresis-based current thresholds of 1.6 A and 1.3 A for the phase add and drop operations, respectively. To trigger the APD control of the VRM, the load current is slowly swept from 1 A to 10 A. The measurement and simulation results are shown in Fig. 12. Overall, the improved simulation model effectively captures the non-linear behavior of VRM caused by APD and shows a good correlation with measured results. Based on the measurement and simulation results shown here, the ability to perform transient analysis using the proposed equation-based VRM modeling method has been successfully validated.

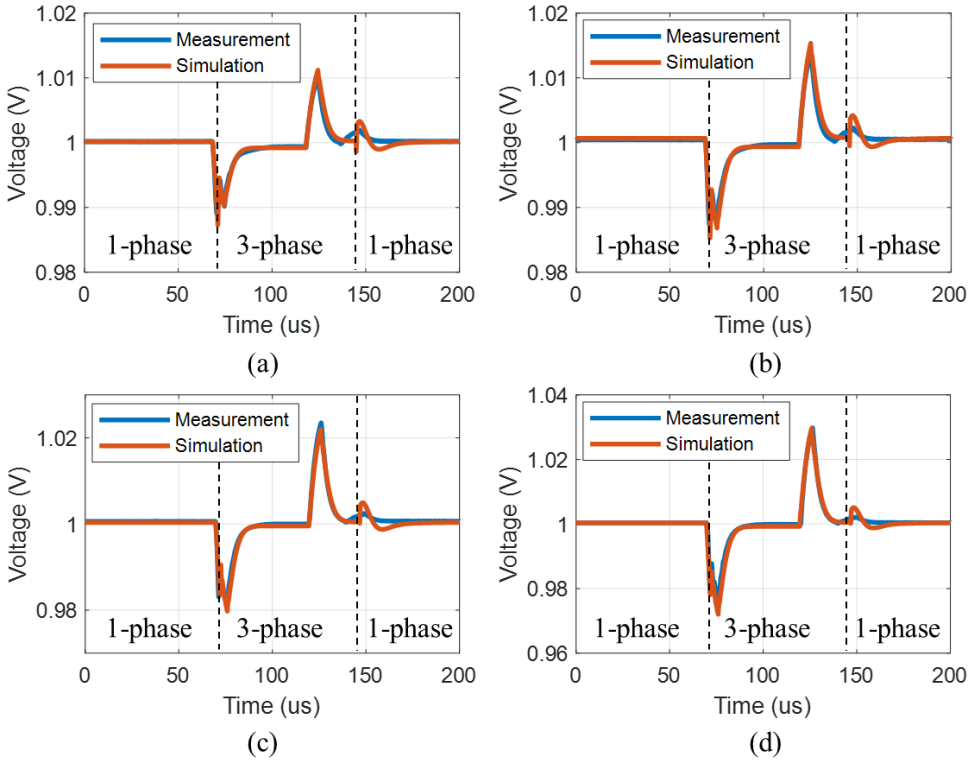

Fig. 12. Correlation results between simulation and measurement for a three-phase VRM with a load of (a) 1–4 A / 5 µs; (b) 1–5 A / 5 µs; (c) 1–8 A / 5 µs; and (d) 1–10 A / 5 µs.

V. Conclusion

In this paper, a SPICE-compatible behavior modeling method for non-linear VRMs is proposed, and parameter-based equations to replicate the complex behaviors of voltage and current control loops are outlined. The parameters are extracted from circuit datasheets, schematics, and measurements. In the SPICE implementation, a VCVS to represent the averaged voltage for the switching node of conventional PWM-based VRMs is used. Finally, the proposed modeling method for practical VRM in mobile applications is validated by comparing against the measurement for single phase operation, 3-phase operation and full multi-phase operation with APD. Other sophisticated features of multiphase VRMs, including load line calibration, dynamic current sharing, and PFM mode, will be introduced in the future work.

References

[1] S. M. Sandler, L. S. Picotest, E. Bogatin, and T. LeCroy, "VRM modeling: A strategy to survive the collision of three worlds," Nov. 2018. [Online]. Available: https://www.signalintegrityjournal.com/articles/1017-vrm-modeling-a-strategy-to-survive-the-collision-of-three-worlds

[2] S. Baek, P. Pun, and A. Agrawal, "Behavioral model of switching dc-dc converter for improving power delivery network design," in Proc. IEEE 62nd Electron. Compon. Technol. Conf., 2012, pp. 926–929.

[3] J. Han, B. Zhang, and D. Qiu, "Unified model of boost converter in continuous and discontinuous conduction modes," IET Power Electron., vol. 9, no. 10, pp. 2036–2043, 2016.

[4] R. E. Griffin, "Unified power converter models for continuous and discontinuous conduction mode," in Proc. IEEE 20th Annu. IEEE Power Electron. Specialists Conf., 1989, pp. 853–860.

[5] S. M. Sandler, "Measurement based VRM modeling," 2017 IEEE 21st Workshop on Signal and Power Integrity (SPI), 2017, pp. 1-4, doi: 10.1109/SaPIW.2017.7944009.

[6] E. Rogers, "SLVA057 - Understanding Buck Power Stages In Switchmode Power Supplies," Texas Instruments, Incorporated, Dallas, TX, 1999.

[7] J. Sun, Y. Yan, H. Wang, E. Chen, K. Wu and J. Fan, "Topology-Based Accurate Modeling of Current-Mode Voltage Regulator Modules for Power Distribution Network Design," in IEEE Transactions on Electromagnetic Compatibility, vol. 64, no. 2, pp. 524-535, April 2022, doi: 10.1109/TEMC.2021.3123338.

[8] A. Huang, J. Sun, H. Kim, Z. Xu, S. Jin, S. Wu, Z. Yang, K. Qui, J. Fan, and C. Hwang, "Transient Behavior Model of Current-Mode Buck Converters for Power Distribution Network Simulation" to be published in IEEE Transactions on Electromagnetic Compatibility.